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PWM CONTROL TECHNIQUE FOR MIGRATION OF VOLTAGE DIPS USING INTERLINE UNIFIED POWER QUALITY CONDITIONER

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ABSTRACT

In this paper PWM Control Technique for migration of voltage dips using Interline Unified power Quality Conditioner. In these control technique we are using two active filters, a series active filter and a shunt active filter (parallel active filter), to control the sinusoidal reference with a source of both voltage and current and also to eliminate the harmonics and unbalance. In iUPQC series active filter (SAF) works as a current source due to this high impedance occurs which is indirectly compensate the harmonics and disturbances of the grid voltage and the load voltage. In iUPQC parallel active filter (PAF) works as a voltage source due to these low impedance occurs which is indirectly compensate the harmonics of grid current and also providing a low impedance path for the harmonic load current. A control technique of pulse width modulation (PWM) to deal with sinusoidal reference for well-known frequency spectrum. In this paper, the proposed iUPQC simulation design control, power flow analysis, and using MATLAB Simulation technique.

Keywords: Active filters SAFs and PAFs, control design with simulation, power line conditioning, interline unified power quality conditioner (iUPQC).

1. INTRODUCTION

In earlier days the major problem in distribution system occurs with increase of nonlinear loads and the power quality is poor at electrical grid. Due to these there is a high harmonic which is distorted the voltage utility at grid and this affect occurs in critical loads from source to load. To

overcome these problem unified power quality conditioner (UPQC) is used in distortion of low harmonic we regulate voltage from the loads and even though it contents harmonic we can undistorted current from the utility grid. A PAF is a non-sinusoidal reference of current source and SAF is non-sinusoidal voltage sources both of them are compensate the harmonic from utility grid voltage and load current. This reference might be complex method which is obtained by the filters to control harmonics. By using this method of complexity of UPQC control technique for both filters without need of harmonic extraction with a sinusoidal reference. The alternative for power quality conditioners was proposed in which line voltage is regulator/conditioner. This conditioner consists of two single-phase current source inverters where the SAF is controlled by a current loop and the PAF is controlled by a voltage loop and both grid current and load voltage are sinusoidal, and therefore, their references are also sinusoidal. In this concept is called "*dual topology of unified power quality conditioner*" (iUPQC), and the control schemes use the $p-q$ theory, for a real time of the positive sequence components of the voltages and the currents. The aim of this paper is to propose a simplified control technique for a dual three-phase topology of a unified power quality conditioner (iUPQC) is to be used in the utility grid connection. In ABC reference the proposed control scheme is developed for the classical control theory without the need for coordinate transformers and digital control implementation. The references to both SAF and PAFs are sinusoidal, dispensing the harmonic extraction of the grid current and load voltage.

II. DUAL UPQC

In order to eliminate the harmonics Dual iUPQC is used and its structure is shown in Fig.1 In the iUPQC, the SAF works as a current source and PAF works as a voltage source both of them synchronized with the grid voltage uses sinusoidal references to the classic topology for both active filters. The high impedance occurs at SAF to indirectly compensate the harmonics, unbalances, and disturbances of the grid voltage the connection transformer voltages are equal to the difference between the grid voltage and the load voltage. In the same way, the PAF indirectly compensates the unbalances, displacement, and harmonics of the grid current, providing a low-impedance path for the harmonic load current.

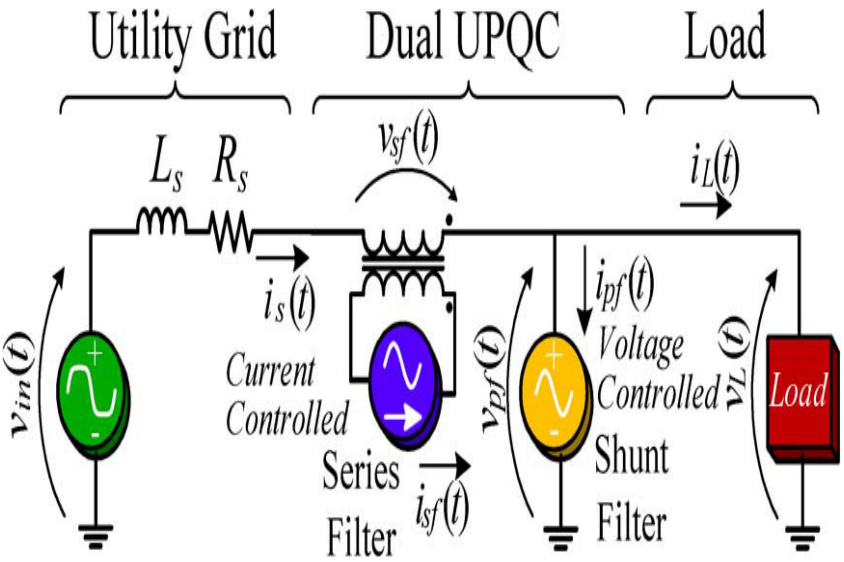

Fig.1 Dual UPQC (iUPQC)

III. POWER CIRCUIT

The power circuit of the proposed scheme of iUPQC is made up of two four-wire three-phase converters connected back to back and their respective output filters, as shown in Fig. 2. Three single-phase transformers are used to connect the SAF to the utility grid, while the PAF is connected directly to the load. Table I shows the specification of the iUPQC. For this work, a commercial back-to-back power module was used, manufactured by SEMIKRON. The passive components are shown in Table II.

TABLE I: DESING SPECIFICATION OF iUPQC

Input line to line RMS voltage	V_{in}=220V
Output nominal power	P_o=2500VA
DC link voltage	V_b=400V
Utility grid frequency	f_{grid}=50Hz
Switching frequency of SAFs and PAFs	f_s=20KHz
Transformer ratio	n=1

TABLE II: COMPONENT SPECIFICATION OF POWER MODULES

Leakage inductance of SAF coupling Transformer	L_{lg}=2.33mH
Transformer ratio of the SAF coupling Transformer	n=1
SAF connection inductance	L_{sf}=650µH
PAF connection inductance	L_{pf}=650µH
DC Link Capacitance	C_b =3mF

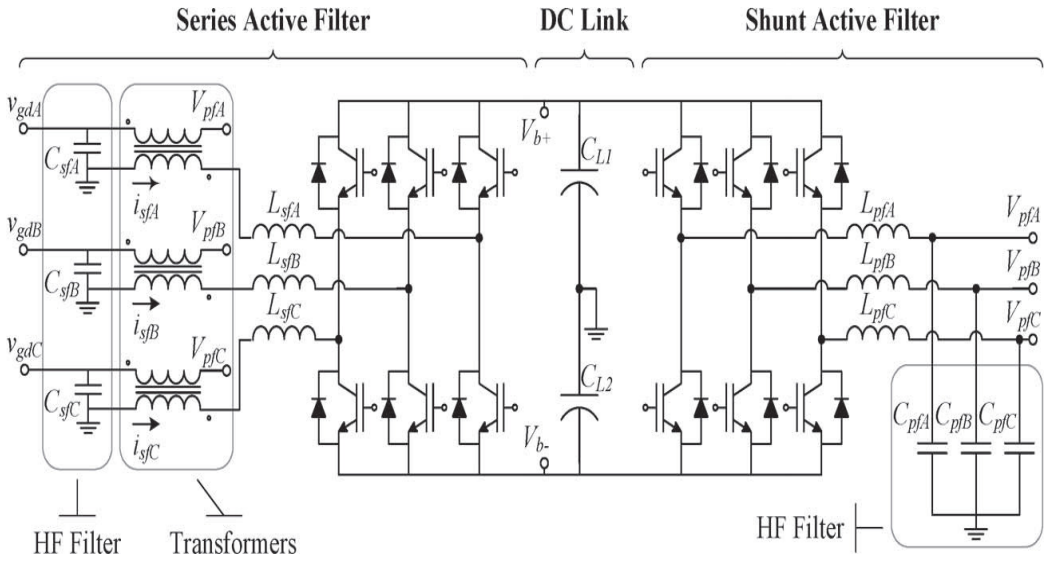

Fig.2 Power circuit of the iUPQC.

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IV. OUTPUT PASSIVE FILTER DESIGN

The iUPQC circuit can be analyzed by a single-phase wiring diagram, as shown in Fig. 3. The utility grid impedance is represented by $Z_s = j\omega L_s + R_s$, while the coupling transformer leakage impedance is represented by $Z_{lg} = j\omega L_{lg} + R_{lg}$, and the voltage sources v_{sc} and v_{pc} represent in the series and shunt filters, and generate a waveform to composed the component and harmonics which are originated from switches. The output passive filters is filtered the high frequency of the iUPQC, for sinusoidal grid currents and load voltages. Fig.4 and Fig.5 output impedance analysis of SAF and PAF. In PAF, the voltage source v_{sc} and the inductance L_{sf}, connected with series as a current source. The equivalent circuits, shows that the PAF output impedance affects the frequency response of the SAF, but when comes to SAF is does not affect the frequency response of the PAF. Therefore, the output passive filter design of iUPQC should be started with the PAF design followed by the SAF design. The high-frequency filter transfer function of the PAF is derived by analyzing the circuit of as shown in Fig.5.

$$\frac{v_{l(s)}}{v_{pc(s)}} = \frac{1}{L_{pf}C_{Pf}} \cdot \frac{1}{s^2 + s\frac{1}{C_{pf}R_L} + \frac{1}{L_{pf}C_{pf}}} \quad (1)$$

The inductor L_{pf} is a power design, and the capacitor C_{pf} is a desired cutoff frequency of the filter. In this design, a 2.9-kHz cutoff frequency was used, resulting in a value of 10μF for the C_{pf} filter capacitor. The PAF frequency response for the nominal load and no load. The high-frequency filter transfer function of the SAF is derived by analyzing the circuit of as shown in Fig. 4

$$\frac{i_s(s)}{v_s(s)} = \frac{n}{sL_{sf} + [n^2[sL_{tg} + R_{tg} + \alpha + \beta]\gamma]} \quad (2)$$

where,

$$\alpha = \frac{sL_{pf}R_L}{s^2L_{sf}C_{pf}R_L + sL_{sf} + R_L} \quad (3)$$

$$\beta = \frac{sL_{rd} + R_{rd}}{s^2L_sC_{sf} + sC_{sf}R_s + 1} \quad (4)$$

$$\gamma = s^2C_{sf}L_s + sC_{sf}R_{lg} + 1 \quad (5)$$

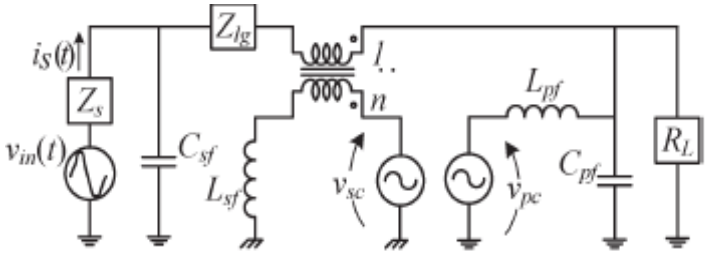


Fig.3 Single-phase wiring diagram of the dual UPQC.

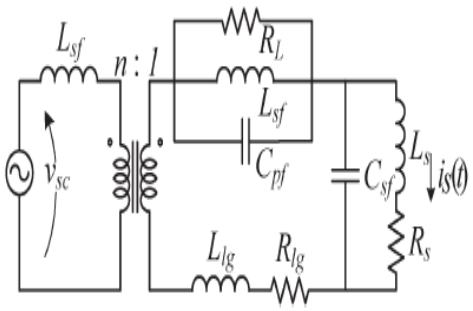


Fig.4 Equivalent circuit as viewed by SAF.

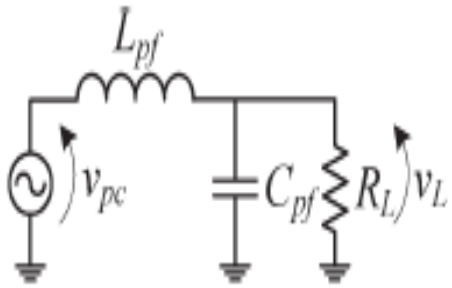


Fig.5 Equivalent circuit as viewed by PAF.

Inductor Lsf *is* a power design, and capacitor C_{sf} is a desired cutoff frequency of the filter is 45-Hz cutoff frequency was used, resulting in a value of 1μF for the C_{sf}. The SAF frequency response for nominal load and no load. It is a low cutoff frequency response by a filter and also it reduce the bandwidth of the SAF, and it contents the harmonic on the grid voltage. The leakage impedance of the coupling transformers is of low-frequency attenuation is undesirable and intrinsic to the characteristic. As per the previous articles, it deal with the same iUPQC control strategy, SAF operates with sinusoidal reference, the output filter of inductor is imposition of voltage by the imposed of SAF current with high frequency and its utility grid voltage harmonics so that it guarantees a sinusoidal current through the filter. The iUPQC is a narrow band frequency control may distort the current drained from the utility grid. The usage of high-power coupling transformers, with low leakage inductance, and the design of higher voltage dc link, allowing the imposition of higher current rate of change on the filter output inductor, is solutions to change the characteristics of the filter attenuation in low frequencies.

V. PROPOSED CONTROL SCHEME

The proposed iUPQC control structure is an ABC reference frame based on the compensation of harmonics, unbalances, disturbances, and displacement. To compensate we are using the SAF has a current loop in order to ensure a sinusoidal grid current which is synchronized with the grid voltage. While PAF has a voltage loop in order to ensure a balanced regulated load voltage with low harmonic distortion. Both of control loops are independently in each active filter. The dc link voltage control is a reference amplitude for the current loop, in the power factor converter control schemes of SAF. With the sinusoidal references for both SAF and PAF controls are generated by a digital signal processor (DSP), and ensure the grid voltage synchronism using a phase locked loop.

A. SAF Control

The SAF control scheme as shown in Fig.6 consists of two voltage loops and three current loops which are identical to grid. In order to control the grid currents which are independently tracking the each grid input reference of phase towards the loops of grid current. The total dc link voltage is regulated to one voltage loop and another voltage loop is avoiding the unbalance towards dc link capacitors. For a low-frequency of total dc voltage control loop and its response which is determined the reference amplitude for the current loops. Due to these we can increase the load to overcoming input of grid current and to decrease the voltage of an dc link supplies of an momentarily towards the resultant active power consumption. The grid current reference is increased by voltage controller to restore the dc link voltage. If the load decrease the dc link voltage of grid current reference also decrease by voltage controller. The neutral point of three phase four wire converter is represent by the circuit is shown in Fig.7 and which its current source is parallel with the dc link impendence and its source is represent by the average charge of current of the dc link. The resistor R_b is infinite ($R_b \rightarrow \infty$); in a circuit to represent instantaneous active power consumption of the dc link which is related to switching period and its null for the utility grid voltage frequency. The average charge current of the dc link is given by

$$I_{eq} = \frac{3}{2} \cdot \frac{n.V_{gdpk}.I_{sfpk}}{V_b} \qquad (6)$$

$$G_{vsf(s)} = \frac{V_{b(s)}}{I_{sf(s)}} = \frac{3}{2} .n. \frac{V_{gdpk}}{V_b} . \frac{1}{\frac{1}{R_b + sC_b}} \qquad (7)$$

Where,

V_{gdpk} Peak of the grid voltage;

V_b DC link voltage;

R_b Load equivalent resistance;

C_b Total dc link equivalent capacitance;

n Transformer ratio

The open loop transfer function (*OLTFs*) is given by

$$OLTFv_{(s)} = G_{vsf(s)} . \frac{K_{vsf}}{F_{isf}} . K_{mfs} \qquad (8)$$

where,

K_{mfs} multiplier gain;
K_{vsf} voltage sensor gain;
K_{isf} current sensor gain.

The K_{mfs} is of multiplier integrated circuit and the peak signal generated by the DSP which is sinusoidal by synchronized.

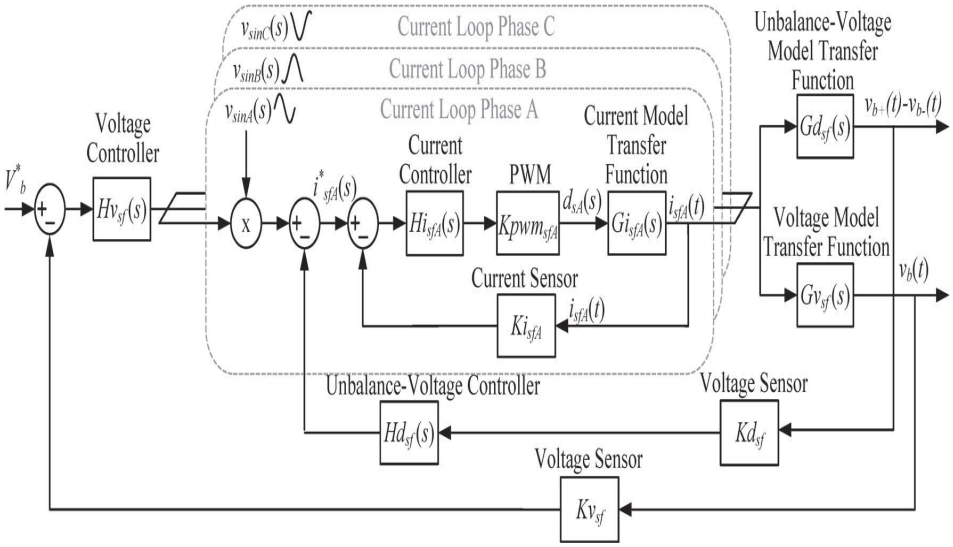


Fig.6 Control block diagram of the SAF controller.

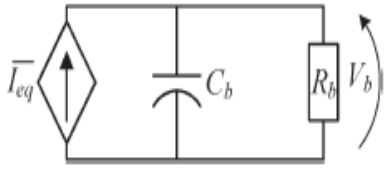


Fig.7 Equivalent circuit of the SAF voltage loop

To regulate these a proportional integral (PI) controller was designed, to ensures a crossover frequency of 4 Hz and a phase margin of 45◦,and its frequency of the total voltage loop, including the open-loop transfer function (*OLTFv*), controller transfer function (Hv_{sf}), and its compensated loop transfer function (*OLTFv*+ Hv_{sf}). The unbalanced-voltage control loop is a low frequency loop level of dc the grid current reference is keep the voltage equilibrium in dc link capacitors. If voltage is unbalance occurs, adds a dc level to the references of the grid currents, and which is both C_{L1} and C_{L2} voltages. To analysis of these function as simplified and the current $i_{sc(t)}$ is a neutral point, and $d(t)$ is a duty cycle. The four wire converter allows the single-phase analysis, where two current sources represent the current on the inverter switches. Through the mesh analysis and by applying Laplace, the unbalanced-voltage loop transfer function is obtained and given by

$$Gd_{sf(s)} = \frac{V_{b+(s)} - V_{b-(s)}}{I_{sc(s)}} = \frac{3}{2.s.C_b} \qquad (9)$$

The open-loop transfer function (*OLTFd*) is given by

$$OLTF_{d(s)} = G_{dsf(s)} * \frac{K_{dsf}}{K_{isf}} \qquad (10)$$

Where,

Kd_{sf} *D*ifferential voltage sensor gain.

To eliminate these a proportional integral (PI) controller was designed, to ensures a crossover frequency of 0.5 Hz and a phase margin of 50◦, and its frequency of differential voltage loop, including the open-loop transfer function ($OLTF_d$), controller transfer function (Hd_{sf}), and compensated loop transfer function ($OLTF_d$ + Hd_{sf}). It consists of three identical current loops,

except for the 120◦ phase displacements from the sinusoidal references of each other. To decoupling the voltage loop and its source on the coupling transformer and the current loop transfer function as shown in Fig.8.The dynamic model of an circuit has an average value related to the switching period. Due to these conditions, the voltage $v_{s(t)}$ and $v_{L(t)}$ are constants. Through small signal analysis and by using Laplace, the current loop transfer function is given by

$$G_{if(s)} = \frac{I_{sc(s)}}{D_{(s)}} = \frac{V_b}{sA_1 + n^2.(R_{(s)} + R_{lg})} \qquad (11)$$

where,

$$A_1 = n^2.(L_s + L_{lg}) + L_{sf} \qquad (12)$$

and

L_s series grid inductance;
R_s series grid resistance;
L_{lg} leakage inductance of the coupling transformer;
R_{lg} series resistance of the coupling transformer.

The open-loop transfer function ($OLTF_i$) is given by

$$OLTFi_{(s)} = G_{isf\,(s)}.K_{pwmsf}K_{isf} \qquad (13)$$

where,
K_{pwmsf} series filter pulse width modulation (PWM) modulator gain and its equal to the inverse peak value of the triangular carrier.

To track these current reference, a proportional integral (PI) controller was designed, to ensures a crossover frequency of 5 kHz and a phase margin of 70◦,and its frequency response of the current loop, including the open-loop transfer function ($OLTF_i$), controller transfer function (Hi_{sf}), and compensated loop transfer function ($OLTF_i + Hi_{sf}$).

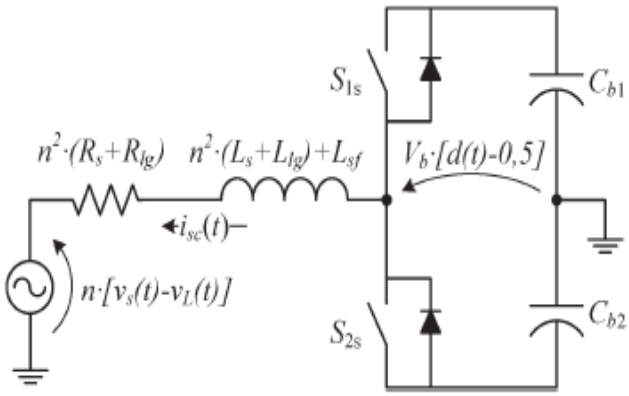


Fig.8 Single-phase equivalent circuit of SAF

B. PAF Control

It is a controlled of shunt active filter as shown in control block diagram Fig.9.The control scheme of three identical load voltage towards feedback loops in 120◦ phase displacements with references of each other. The transfer function is analysis through a single-phase equivalent circuit of voltage loop as shown in Fig.10.We are using average values related to the switching period and it for a small signal analysis and by using Laplace, the voltage loop transfer function is given by

$$G_{vpf(s)} = \frac{V_b}{L_{pf} C_{pf}} \cdot \frac{1}{s^2 + s(\frac{1}{C_{pf} R_L}) + \frac{1}{L_{pf} C_{pf}}} \quad (14)$$

where,

$$G_{vpf(s)} = \frac{V_{L(s)}}{D_{(s)}}$$

The open-loop transfer function ($OLTFv_{pf}$) is given by

$$OLTFv_{(s)} = G_{vsf(s)} . K_{pwmpf} K_{vpf} \quad (15)$$

Where,

K_{pwmpf} shunt filter PWM modulator gain.

In order to these additional (PID) pole controller was designed, to ensures a crossover frequency in a proportional integral derivate of 4 kHz and a phase margin of 35◦ to track the voltage reference. The voltage loop frequency response, including the open-loop transfer function ($OLTFv_{pf}$), controller transfer function (Hv_{pf}), and compensated loop transfer function ($OLTFv_{pf} + Hv_{pf}$).

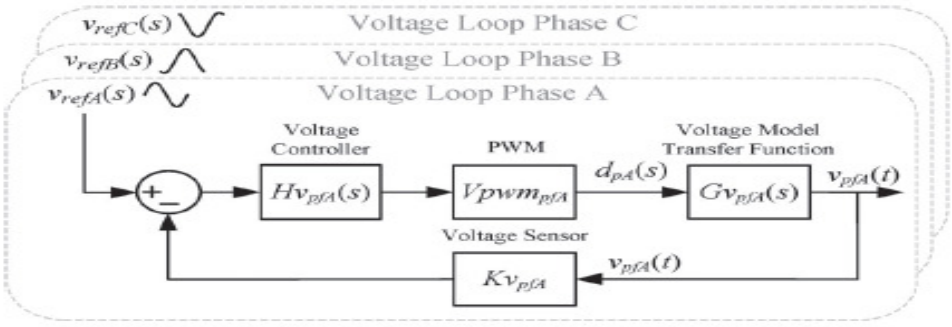


Fig.9 Control block diagram of the PAF voltage loop.

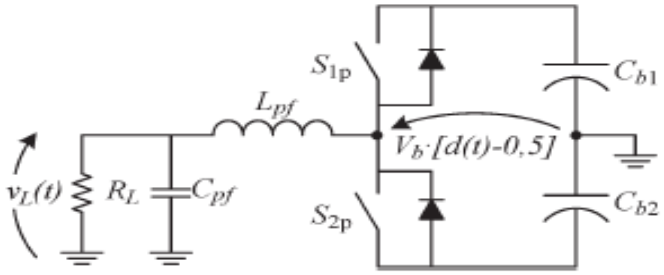
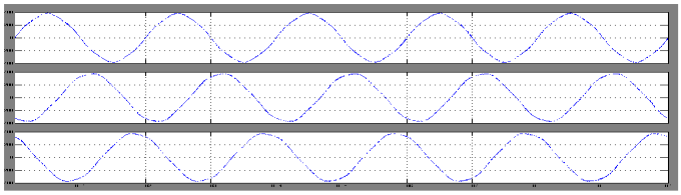


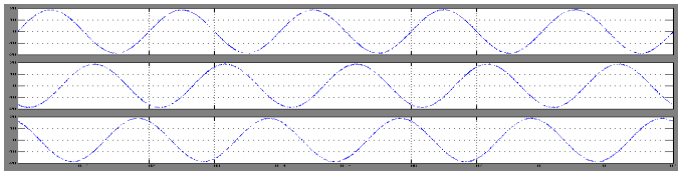
Fig.10 Single-phase equivalent circuit of PAF.

VII. RESULT

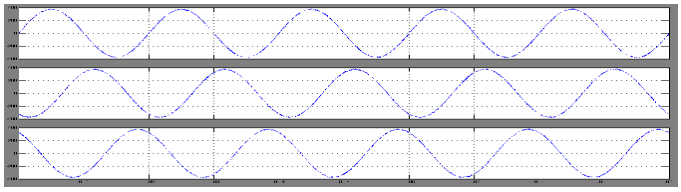
The result is obtained through PWM control technique for migration of voltage dips using interline unified power quality conditioner-iUPQC. From grid source to load we are eliminating the harmonics using both filters and injecting the dip voltage and compensating load with DC link current load to discrete the RMS voltage. Hence the result output is sinusoidal from grid source to load is without harmonics.



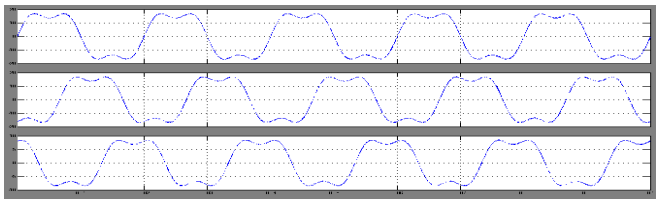
(a) Voltage Source: Vabc.



(b) Current Source: Iabc.

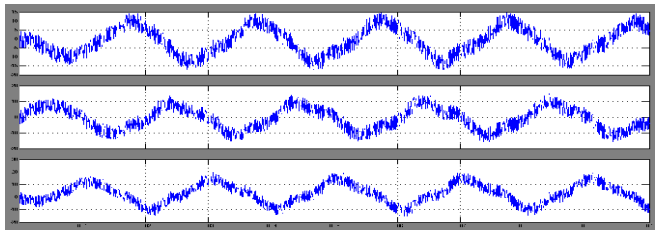


(c) Voltage Load:-Vabcl.

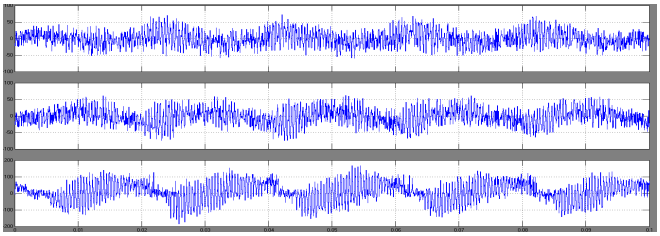


(c) Current Load:-Iabcl.

Fig.11. (a), (b), (c) Waveform of source and load voltages (100V/div and 5ms/div) and source and load current (10A/div and 5ms/div).

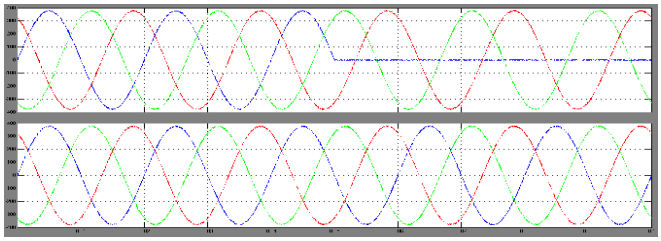


(a) PAF Current Frequency affected harmonics:-IFabc.

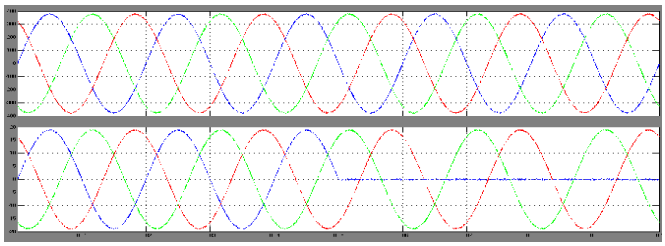


(b) SAF Voltage Frequency affected harmonics:-VFabc.

Fig.12. (a) Waveform of PAF current (6A/div and 5ms/div). (b) SAF voltage (30V/div and 2.5ms/div).

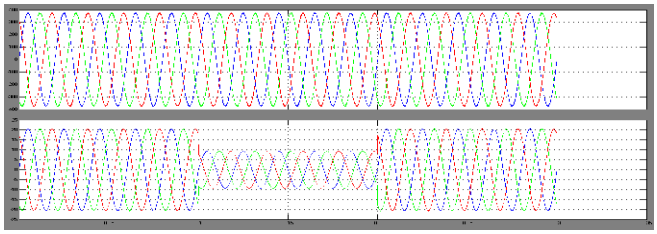


(a) Waveform of three phase source voltages with voltage dip in phase A and load voltage.

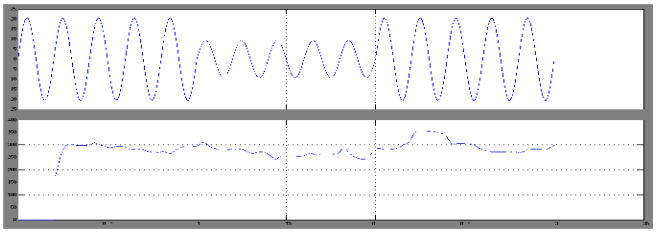


(b) Waveform of three phase load current and source currents with voltage dip in phase A.

Fig.13. (a) Waveform of three phase source voltages and load voltages (100V/div and 5ms/div) during a voltage dip in phase A. (b) Waveform of three phase load voltages (100V/div and 10ms/div) and source currents (5A/div and 10ms/div) during a voltage dip in phase A.



(a) Waveform of three phase load voltages and load currents:-Vabcl, Iabcl.



(b) Waveform of three phase load current Iabcl with DC link voltages with discrete RMS.

Fig.14. (a) Waveform of three phase load voltages (100V/div and 5ms/div) and load current (5A/div and 5ms/div) during a load step from 100% to 50% and 50% to 100%. (b) Waveform of DC link voltages (100V/div and 50ms/div) and load current (5A/div and 50ms/div) during a load step from 100% to 50%.

VIII. CONCLUSION

The results is through with iUPQC using Matlab Simulation Technique in ABC reference frame and using series active filter to compensate the harmonics from nonlinear load current and a sinusoidal voltage form the load is without reference harmonic and at source side if load steps and due to these there is disturbance occurs to eliminate we are using parallel active filter at source voltage . A proposed scheme of iUPQC in ABC reference frame to control of both the active filters

and their control loops are generated by a digital signal processor (DSP) and to related to other proposed controls its utilization is better for a sinusoidal reference and to eliminate the harmonic from source to load using different technique to synchronism with grid voltage. While coming towards its application iUPQC, the high impedance occurs at SAF. The non-interference of leakage impedance voltage towards the SAF and non-sinusoidal current source is compensating the load voltage which is directly controlled by the PAF. Due to these the leakage impendence of SAF at other hand decreases with bandwidth and its response frequency under grid voltage. Both the active filters from source to load are dip by the RMS voltage in phase A to eliminate the harmonics from grid source voltage to load current. Thus the result is validated and its proposed scheme of ABC reference of iUPQC control method is used in synchronized sinusoidal reference.

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